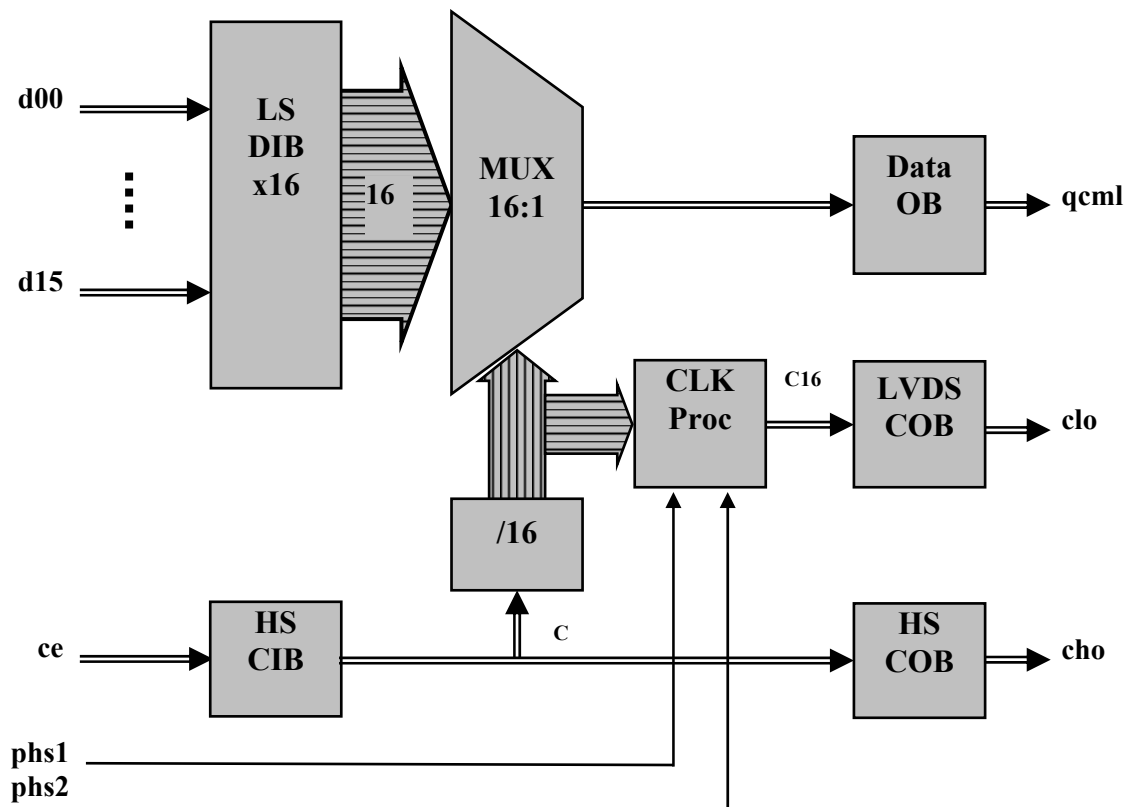


## ASNT1011 (ASNT1022) 16:1 Digital MUX

- Digital 16 to 1 multiplexer (MUX).
- Broadband serializer operates seamlessly from DC to 14Gbps.
- LVDS compliant input data buffers.
- Full rate clock output.
- Clock-divided-by-16 LVDS output buffer with 90°-step phase selection.
- Single +3.3V power supply.
- Industrial temperature range.
- Low power consumption of 600mW at 14Gbps.
- Available in standard 100-pin QFN package (12mm x 12mm).

### DESCRIPTION



*Fig. 1. Functional Block Diagram.*



ASNT1011 is a low power and high-speed digital 16 to 1 multiplexer (MUX). The MUX functions seamlessly over data rates ( $f_{bit}$ ) ranging from DC to 14Gbps.

The main function of ASNT1011 is to multiplex 16 parallel data channels running at a bit rate of  $f_{bit}/16$  into a high speed serial bit stream running at  $f_{bit}$ . It provides a high-speed output data channel for point-to-point data transmission over a controlled impedance media of 50 $\Omega$ . The transmission media can be a printed circuit board or copper coaxial cables. The functional distance of the data transfer is dependent upon the attenuation characteristics of the transportation media and the degree of noise coupling to the signaling environment.

During normal operation, the serializer's low-speed input buffer (LS DIBx16) accepts external 16-bit wide parallel data words "d00"- "d15" through 16 differential LVDS inputs and delivers them to the multiplexer's core (MUX16:1) for serialization. Full rate clock must be provided by an external source ("ce") to the high-speed clock input buffer (HS CIB) where it is routed to the high speed clock output buffer (HS COB) and the internal divider-by-16 (/16). The divider provides signaling for MUX16:1 and produces full rate clock divided-by-16 "C16" for the low speed LVDS compliant clock output buffer (LVDS COB). The phase of "clo" can be modified by 90° increments by utilizing pins "phs1" and "phs2" and the clock processing block (CLK Proc).

The serialized words are transmitted as 2-level signals "qcml" by a differential CML output buffer (Data OB). A full-rate clock "cho" is transmitted by a similar CML buffer HS COB in parallel with the high-speed data. The clock and data outputs are well phase matched to each other resulting in very little relative skew over the operating temperature range of the device. Both output stages are back terminated with on-chip 50 $\Omega$  resistors.

The serializer uses a single +3.3V power supply and is characterized for operation from -25°C to 125°C of junction temperature.

## LS DIBx16

The Low-Speed Data Input Buffer (LS DIBx16) consists of 16 proprietary universal input buffers (UIBs) that exceed the LVDS standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. UIB is designed to accept differential signals with amplitudes above 60mV peak-to-peak (p-p), DC common mode voltage variation between the negative (vee) and positive (vcc) supply rails, and AC common mode noise with a frequency up to 5MHz and voltage levels ranging from 0 to 2.4V. It can also receive single-ended signals with amplitudes above 60mV p-p and threshold voltages between vee and vcc. The input termination impedance is set to 100 $\Omega$  differential.

## HS CIB

The High-Speed Clock Input Buffer (HS CIB) can process an external CML clock signal "ce" with frequencies from DC to 15GHz. It can also accept a single-ended signal to "cep/cen" with a threshold voltage applied to the unused "cen/cep" pin. HS CIB can handle input signal amplitudes between 200mV and 1.2V p-p differential or single-ended. The buffer utilizes on-chip single-ended termination of 50 $\Omega$  to vcc for each input line.



### /16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. High-speed clock “C” is fed into the first divide-by-2 circuit that generates half rate clock “C2”. “C2” is routed internally to the next divide-by-two circuit and outside of the block to MUX16:1. Other divided down clock signals are formed and routed to MUX16:1 in similar fashion. “C16” is passed on to LVDS COB to become the output low speed clock signal “clo”.

### MUX16:1

The 16 to 1 Multiplexer (MUX16:1) utilizes a tree type architecture that latches the incoming data on the negative edge of the “C16” clock signal that is supplied by /16. The 16-bit wide data word is subsequently multiplexed and delivered to Data OB as a single serial data stream running at a data rate up to 14Gbps. The latency of this circuit block is equal to roughly one period of “C16”. MUX16:1 is configured so “d00” is treated as the MSB.

### Data OB

The Data Output Buffer (Data OB) receives high-speed serial data from MUX16:1 and converts it into the CML output signal “qcml” with a single ended swing of 600mV. The buffer requires 50Ohm external termination resistors connected between “vcc” and each output to match its internal 50Ohm resistors and can operate at a data rate up to 15Gbps.

### HS COB

The High Speed Clock Output Buffer (HS COB) utilizes the same termination scheme as Data OB and can operate at a frequency up to 15GHz while producing a single-ended CML output swing of 600mV.

### CLK Proc

By utilizing the CMOS control pins “phs1” and “phs2”, the phase of “clo” can be altered in accordance with the table below.

“phs1”	“phs2”	C16 phase
V <sub>EE</sub> (default)	V <sub>EE</sub> (default)	270°
V <sub>EE</sub>	V <sub>CC</sub>	180°
V <sub>CC</sub>	V <sub>EE</sub>	90°
V <sub>CC</sub>	V <sub>CC</sub>	0°

### LVDS COB

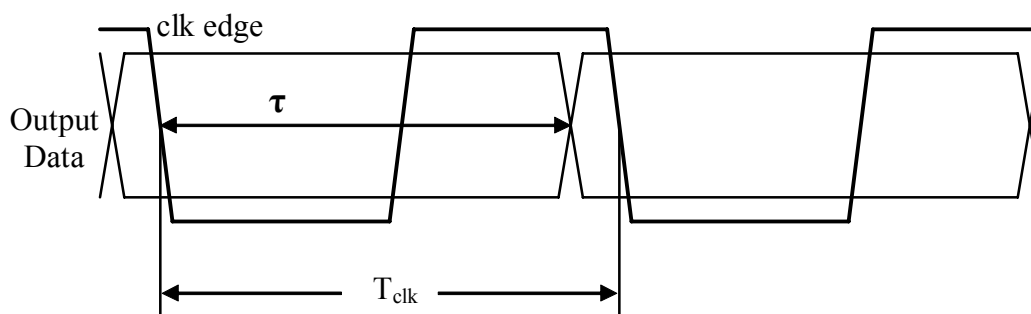
The LVDS Clock Output Buffer (LVDS COB) receives “C16” and converts it into a LVDS output signal “clo”. The proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2GHz with a low power consumption level of 30mW. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

## Output Timing

The phase relation between the output data “qcm1” and full rate output clock “cho” is specified in Table 1 and illustrated by Fig. 2.

*Table 1. Output Data-to-Clock Phase Difference*

Junction temperature, °C	$\tau$ , ps	
	Min.	Max.
-25	77	80
50	82	86
125	87	91



*Fig. 2. Output Timing Diagram*

## TERMINAL FUNCTIONS

The description of the package pins is presented in the table below.

TERMINAL			DESCRIPTION
Name	No.	Type	
<b>High-Speed I/Os</b>			
cep	31	Input	CML differential external clock inputs with internal SE 50Ohm termination to “vcc”.
cen	30		
chop	37	Output	CML differential clock outputs. Require external SE 50Ohm termination to “vcc”.
chon	36		
qcm1p	43	Output	CML differential data outputs. Require external SE 50Ohm termination to “vcc”.
qcm1n	42		
<b>Controls</b>			
phs1	57	LS In.,	Low-speed output clock phase selection (default: both low).
phs2	56	CMOS	
<b>Low-Speed I/Os</b>			
clop	48	Output	LVDS clock outputs. Can transmit four different clock phases as defined by “phs1” and “phs2”.
clon	47		
d00p	61	Input	
d00n	62		



d01p	64	LVDS data inputs.
d01n	65	
d02p	67	
d02n	68	
d03p	70	
d03n	71	
d04p	76	
d04n	77	
d05p	79	
d05n	80	
d06p	82	
d06n	83	
d07p	85	
d07n	86	
d08p	88	
d08n	89	
d09p	90	
d09n	91	
d10p	93	
d10n	94	
d11p	96	
d11n	97	
d12p	99	
d12n	100	
d13p	5	
d13n	6	
d14p	8	
d14n	9	
d15p	11	
d15n	12	

***Supply and Termination Voltages***

<b>Name</b>	<b>Description</b>	<b>Pin Number</b>
vcc	Positive power supply. (+3.3V)	1, 4, 7, 10, 13, 16, 26, 29, 32-35, 38-41, 44, 45, 49, 52, 55, 60, 63, 66, 69, 72, 75, 78, 81, 84, 87, 92, 95, 98.
vee	Negative power supply. (GND or 0V)	3, 17-20, 24, 25, 27, 28, 50, 51, 58, 73.
nc	Unconnected pin.	2, 14, 15, 21-23, 46, 53, 54, 59, 74.



## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b><u>General Parameters</u></b>					
V <sub>CC</sub>	+3.14	+3.3	+3.47	V	±5%
V <sub>EE</sub>		0.0		V	
Power consumption		660		mW	
Junction temperature	-25	50	125	°C	
<b><u>LS Input Data (d00-d15)</u></b>					
Data Rate	0.0	875	937.5	Mbps	
Differential Swing	0.06		0.8	V	Peak-to-peak
CM Voltage Level	V <sub>EE</sub>		V <sub>CC</sub>	V	
<b><u>HS Input Clock (ce)</u></b>					
Frequency	0.0	14	15	GHz	
Swing (Diff or SE)	0.2		1.2	V	Peak-to-peak
CM Voltage Level	V <sub>CC</sub> -0.8		V <sub>CC</sub>	V	
Duty Cycle	40%	50%	60%		
<b><u>HS Output Data (qcml)</u></b>					
Data Rate	0.0	14	15	Gbps	
Logic "1" level		V <sub>CC</sub>		V	
Logic "0" level		V <sub>CC</sub> -0.6		V	
Jitter		12		ps	Peak-to-peak @12.5Gb/s
<b><u>HS Output Clock (cho)</u></b>					
Frequency	0.0	14	15	GHz	
Logic "1" level		V <sub>CC</sub>		V	
Logic "0" level		V <sub>CC</sub> -0.6		V	
Jitter		6		ps	Peak-to-peak @12.5GHz
Duty Cycle		50%			
<b><u>LS Output Clock (clo)</u></b>					
Frequency	0.0	875	937.5	MHz	
Interface		LVDS			Meets the IEEE Std.
<b><u>CMOS Control Inputs</u></b>					
Logic "1" level	V <sub>CC</sub> -0.4			V	
Logic "0" level			V <sub>EE</sub> +0.4	V	

## PACKAGE INFORMATION

The chip is packaged in a standard 100-pin QFN package. The package's mechanical information is available on the company's [website](#).