

ASNT2011 (ASNT2032) 1:16 Digital DMUX

- Digital 1:16 demultiplexer (DMUX).
- Broadband deserializer operates seamlessly from DC to 15Gbps.
- LVDS output data buffers that feature a low-power proprietary architecture.
- Clock-divided-by-16 LVDS output buffer with 90°-step phase selection.
- Single +3.3V power supply.
- Industrial temperature range.
- Low power consumption of 730mW at 15Gbps.
- Available in standard 100-pin QFN package (12mm x 12mm).

DESCRIPTION

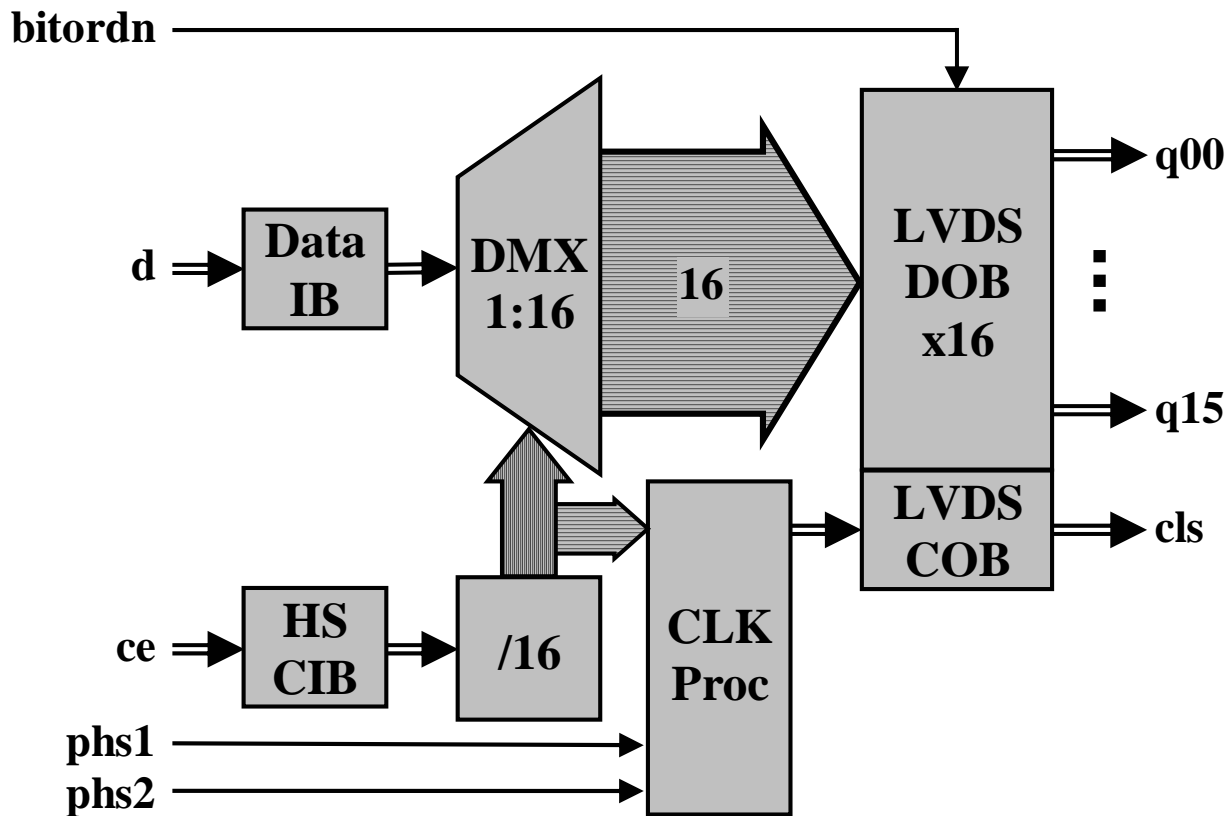


Fig. 1. Functional Block Diagram.



ASNT2011 is a low power and high-speed digital 1 to 16 demultiplexer (DMUX). The DMUX can function seamlessly over input data rates (f_{bit}) ranging from DC to 15Gbps.

The main function of ASNT2011 is to demultiplex a serial input data channel “d” running at a bit rate of f_{bit} into 16 parallel data channels “q00-q15” running at a bit rate of $f_{bit}/16$. The high sensitivity data input buffer (Data IB) ensures accurate operation for input data signal amplitudes greater than 40mV p-p differential or single-ended. It provides on-chip 50Ohm termination and is designed to be driven by devices with 50Ohm source impedance.

During normal operation, the received serial input data is latched into the tree-type demultiplexer (DMX1:16) and subsequently deserialized and delivered to the demultiplexer’s output as 16-bit wide low-speed parallel words. Utilizing pin “bitordn”, the deserializer can designate either “q00” or “q15” as the MSB thus simplifying the interface between ASNT2011 and a following ASIC.

Full rate clock must be provided by an external source “ce” to the high-speed clock input buffer (HS CIB) where it is routed to the internal divider-by-16 (/16). The divider provides signaling for DMX1:16 and produces full rate clock divided-by-16 “C16” for the low speed LVDS compliant clock output buffer (LVDS COB). The phase of “cls” can be modified by 90° increments by utilizing pins “phs1” and “phs2” and the clock processing block (CLK Proc).

Sixteen proprietary low-power LVDS output data buffers (LVDS DOBx16) are used to deliver the 16 data output signals “q00-q15” while a similar LVDS clock output buffer (LVDS COB) outputs the low-speed clock signal “cls”. The buffers satisfy all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995 while only consuming 30mW each.

The deserializer uses a single +3.3V power supply and is characterized for operation from -25°C to 125°C of junction temperature.

Data IB

The Data Input Buffer (Data IB) can process an input CML data signal “d” with bit rates from DC to 15Gbps. It can also accept a single-ended signal to one of its pins with a threshold voltage applied to the unused pin. Data IB can handle input signal amplitudes between 40mV and 1.2V peak to peak (p-p) differential or single-ended. The buffer utilizes on-chip single-ended termination of 50Ohm to vcc for each input line.

HS CIB

The High-Speed Clock Input Buffer (HS CIB) can process an external CML clock signal “ce” with frequencies from Dc to 15GHz. It can also accept a single-ended signal to one of its pins with a threshold voltage applied to the unused pin. HS CIB can handle input signal amplitudes between 200mV and 1.2V p-p differential or single-ended. The buffer utilizes on-chip single-ended termination of 50Ohm to vcc for each input line.

/16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. The high-speed clock delivered by HS CIB is fed into the first divide-by-2 where its output is routed internally to



the next divide-by-two circuit and outside of the block to DMX1:16. Other divided down clock signals are formed and routed to DMX1:16 in similar fashion. Full rate clock divided-by-16 “C16” is passed on to CLK Proc for additional phase adjustment.

DMX1:16

The 1 to 16 Demultiplexer (DMX1:16) utilizes a tree type architecture that latches in the data stream from Data IB on both edges of a half rate clock signal supplied by /16. The high speed data signal is subsequently demultiplexed down and delivered to LVDS DOBx16 in parallel fashion as 16-bit wide words running at a data rate up to 937.5Mbps.

CLK Proc

By utilizing the CMOS control pins “phs1” and “phs2”, the phase of “cls” can be altered in accordance with the table below.

“phs1”	“phs2”	C16S phase
V _{EE} (default)	V _{EE} (default)	270°
V _{EE}	V _{CC}	180°
V _{CC}	V _{EE}	90°
V _{CC}	V _{CC}	0°

LVDS DOBx16

The LVDS Data Output Buffer (LVDS DOBx16) accepts 16-bit wide words from DMX1:16 and converts them into LVDS output signals. Each proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at bit rates up to 2Gb/s with a low power consumption level of 30mW. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

LVDS COB

The LVDS Clock Output Buffer (LVDS COB) receives “C16” from CLK Proc and converts it into the LVDS output signal “cls”. The proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2GHz with a low power consumption level of 30mW. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. When “bitorder”=0 (default), “q00” is the MSB and when “bitorder”=1, “q15” is designated the MSB.



TERMINAL FUNCTIONS

The description of the package pins is presented in the table below.

TERMINAL			DESCRIPTION
Name	No.	Type	
Low-Speed I/Os			
q00n	12	Output	LVDS data outputs.
q00p	11		
q01n	9		
q01p	8		
q02n	6		
q02p	5		
q03n	100		
q03p	99		
q04n	97		
q04p	96		
q05n	94		
q05p	93		
q06n	91		
q06p	90		
q07n	89		
q07p	88		
q08n	86		
q08p	85		
q09n	83		
q09p	82		
q10n	80		
q10p	79		
q11n	77		
q11p	76		
q12n	71		
q12p	70		
q13n	68		
q13p	67		
q14n	65		
q14p	64		
q15n	62		
q15p	61		
clsp	14	Output	LVDS clock outputs. Can transmit four different clock phases as defined by "phs1" and "phs2".
clsn	15		



High-Speed I/Os

dp	43	Input	CML differential data inputs with internal SE 50 Ω termination to “vcc”.
dn	42		
cep	37	Input	CML differential clock inputs with internal SE 50 Ω termination to “vcc”.
cen	36		

Controls

phs1	57	LS In., CMOS	Low-speed output clock phase selection (default: both low).
phs2	56		
bitordn	18	LS In., CMOS	Output bit order selection (active: high, q15 is MSB; default: low, q00 is MSB).

Supply and Termination Voltages

Name	Description	Pin Number
vcc	Positive power supply. (+3.3V)	1, 7, 10, 13, 16, 29, 32-35, 38-41, 44, 45, 49, 52, 55, 60, 63, 66, 69, 72, 78, 81, 84, 87, 92, 95, 98.
vee	Negative power supply. (GND or 0V)	3, 17, 25, 50, 51, 58.
nc	Unconnected pin.	2, 4, 19-24, 26-28, 30, 31, 46-48, 53, 54, 59, 73-75.



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<u>General Parameters</u>					
V _{CC}	+3.14	+3.3	+3.47	V	±5%
V _{EE}		0.0		V	
Power consumption		730		mW	
Junction temperature	-25	50	125	°C	
<u>HS Input Data (d)</u>					
Data Rate	0	15	17	Gbps	
Swing p-p (Diff or SE)	0.04		1.2	V	Peak-to-peak
CM Voltage Level	V _{CC} -0.8		V _{CC}	V	
<u>HS Input Clock (ce)</u>					
Frequency	0.0	15	17	GHz	
Swing p-p (Diff or SE)	0.2		1.2	V	Peak-to-peak
CM Voltage Level	V _{CC} -0.8		V _{CC}	V	
Duty Cycle	40%	50%	60%		
<u>LS Output Data (q00-q15)</u>					
Data Rate	0.0	937.5	1063	Mbps	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
<u>LS Output Clock (cls)</u>					
Frequency	0.0	937.5	1063	MHz	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
<u>CMOS Control Inputs/Outputs</u>					
Logic "1" level	V _{CC} -0.4			V	
Logic "0" level			V _{EE} +0.4	V	
<u>Timing Parameters</u>					
"cls" to "q0-q15" delay variation		±2.5%			Over the full temperature range

PACKAGE INFORMATION

The chip is packaged in a standard 100-pin QFN package. The package's mechanical information is available on the company's [website](#).