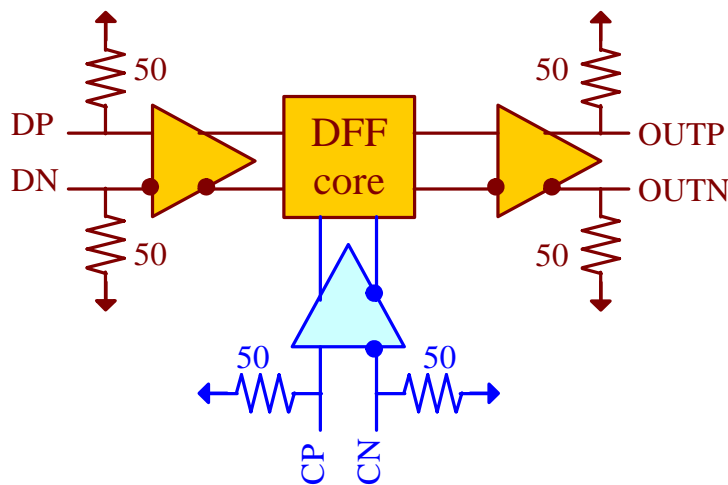
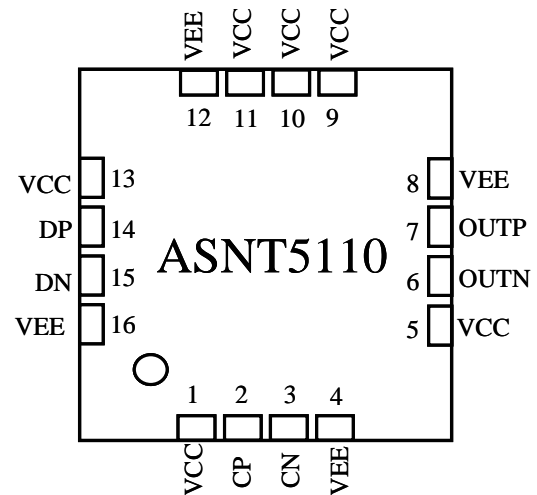


ASNT5110/5011-PQD 14Gbps D-Type Flip-Flop

- High speed broadband D-Type Flip-Flop for data retiming with full rate clock.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 14GHz analog input bandwidth for both clock and data inputs.
- 7ps set-up/hold time capability.
- 88% clock phase margin for retiming of data input eye.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with 400mV single-ended swing.
- Single ±3.3V power supply.
- Power consumption: 300mW.
- Fabricated in SiGe for high performance, yield, and reliability.
- Standard MLF/QFN 16-pin package.



Functional Block Diagram



Package Pins

DESCRIPTION

The temperature stable ASNT5110-PQD SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. ASNT5110-PQD can sample an up to 14Gbps data signal with an up to 14GHz clock source to create a 14Gbps retimed NRZ data output. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single ±3.3V power supply.



TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	(NO.)		
vcc	1,5,9,10,11,13	PS	Power Supply: 3.3V / 0V
vee	4,8,12,16	PS	Power Supply: 0V / -3.3V
dp	14	Input	Differential CML high-speed data signal inputs
dn	15		
cp	2	Input	Differential CML high-speed clock signal inputs
cn	3		
outp	7	Output	Differential CML high-speed data signal outputs
outn	6		

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	0.0 / -3.3	-3.5	V	±6%
VCC	3.1	3.3 / 0.0	3.5	V	±6%
IEE		90		mA	
Power		300		mW	
Junction Temp.	-25	50	125	°C	
Input Data (d)					
Frequency	0.0		14	Gbps	
CM Level	V _{cc} -0.8	V _{cc} -0.3	V _{cc} +0.3	V	
SE Swing	50	300	800	mV	Peak-to-peak
Input Clock (c)					
Frequency	0.0		14	GHz	
CM Level	V _{cc} -0.8	V _{cc} -0.3	V _{cc} +0.3	V	
SE Swing	50	300	800	mV	Peak-to-peak
Duty Cycle	40%	50%	60%		
Output Data (out)					
Frequency	0.0		14	Gbps	
CM Level	V _{cc} -0.3	V _{cc} -0.2	V _{cc} -0.1	V	
SE Swing	380	400	420	mV	Peak-to-peak
Rise/Fall Times			<20	ps	20%-80%
Jitter			<5	ps	Peak-to-peak
Clock Phase Margin	85%	88%	90%		

PACKAGE INFORMATION

The chip is packaged in a standard 16-pin QFN package. The package's mechanical information is available on the company's [website](#).