ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275

Offices: 310-377-6029 / 310-803-9284 Fax: 310-377-9940
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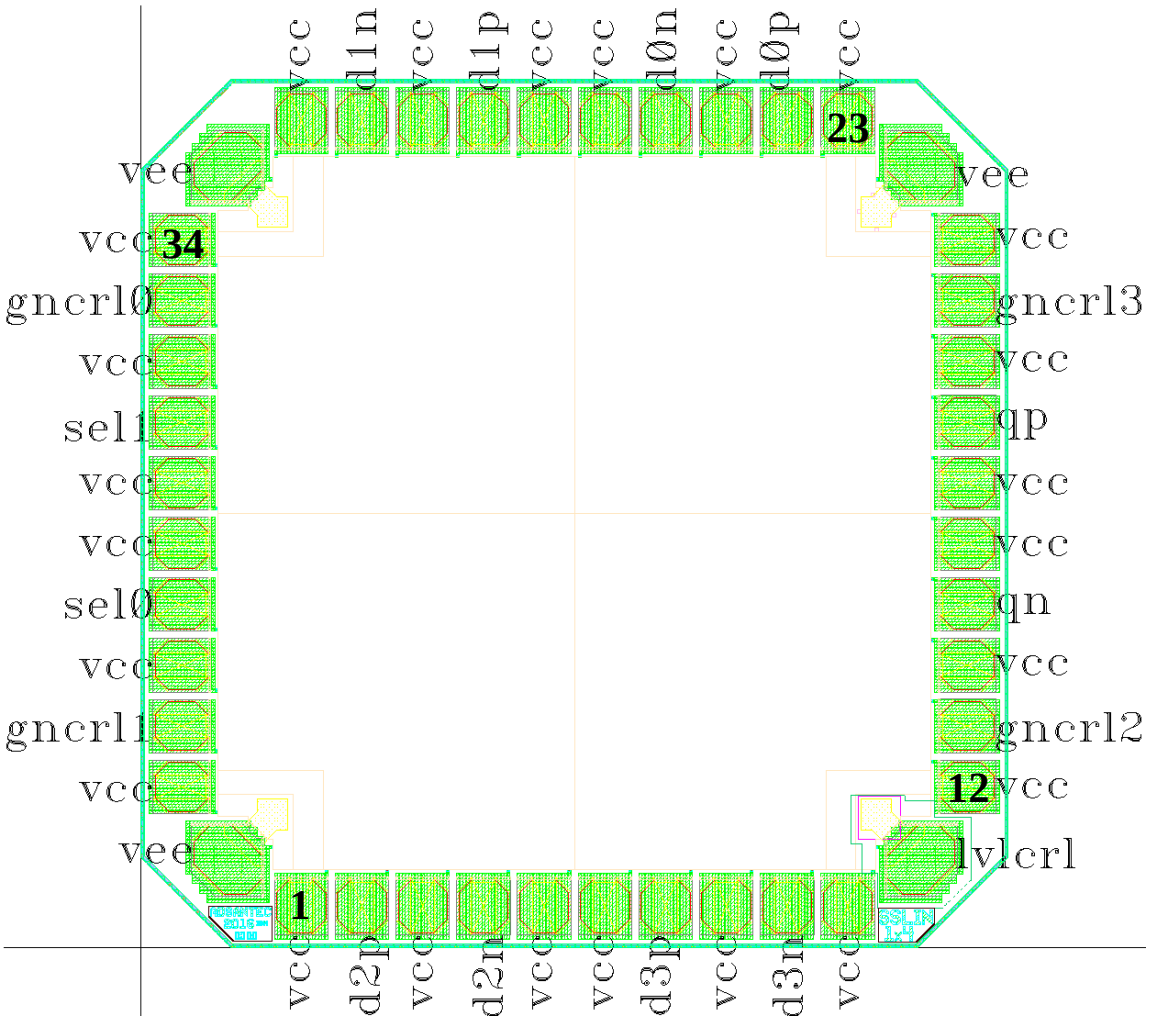
ASNT6161-BD
DC-17*GHz* Analog Signal Selector 1-of-4

- DC to 17*GHz* broadband operation
- Four differential CML-type input ports and one differential CML-type output port
- Temperature-stabilized differential gain of approximately 0*dB*
- 1*dB* compression point of 0*dBm*
- DC-to-1*GHz* broadband channel selector ports
- Low jitter and limited temperature variation over industrial temperature range
- Single +4.5*V* or -4.5*V* power supply
- Power consumption: 2.1*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Pad frame with 44 pads



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DESCRIPTION

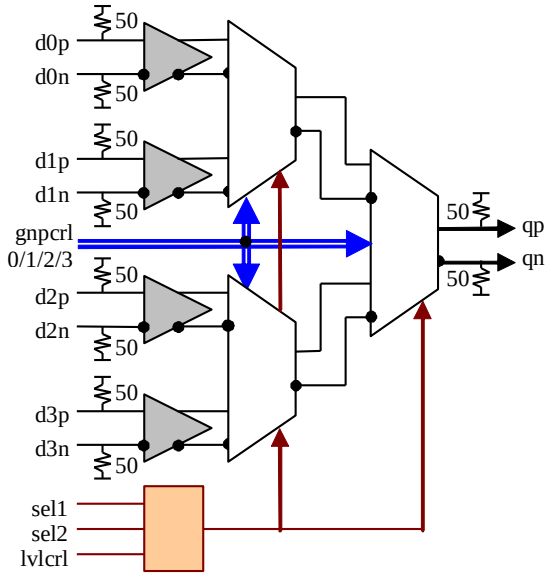

Fig. 1. Functional Block Diagram

The temperature stable ASNT6161-BD analog signal selector 1-of-4 is intended for use in high-speed systems. The IC shown in Fig. 1 can deliver one of four different broad-band analog differential signals d0p/d0n, d1p/d1n, d2p/d2n, and d3p/d3n to its differential output qp/qn with a nominal gain of 0*dB*. The gain can be fine-tuned using the 4-pin control port gncrl0/1/2/3 with accuracy of 0.5*dB* as shown in Table 1.

Table 1. Gain Control

gncrl3	gncrl2	gncrl1	gncrl0	Gain, *dB*	Comments
0	0	0	0	-2.0	
0	0	0	1	-1.5	
0	0	1	0	-1.0	
0	0	1	1	-0.5	
0	1	0	0	0.5	
0	1	0	1	1.0	
0	1	1	0	1.5	
0	1	1	1	2.0	
1	X	X	X	0	default state 1111

The active input selection is performed through the external high-speed dual port sel1/sel2. The selection logic is shown in Table 2.

Table 2. Channel Selection

sel1	sel2	Input connected to output
0	0	d0 (default state)
0	1	d1
1	0	d2
1	1	d3

The port accepts 3.3*V* CMOS signals referenced to either vee or vcc depending on the state of the lvlcrl port: lvlcrl="1" sets low levels for sel1/sel2 to vee, lvlcrl="0" or not connected sets high levels for sel1/sel2 to vcc.

The part's I/Os support the CML-type interface with on chip 50*Ohm* termination to vcc, and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance. In particular, the specified output common-mode voltage level is guaranteed only in case of external single-ended 50*Ohm* DC termination to vcc.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V* = ground), or a positive supply (vee = 0.0*V* = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. In any case, the input common mode voltage level is shifted down from vcc by a certain voltage of ΔV_{ICM} as specified in ELECTRICAL CHARACTERISTICS. To have the input common mode voltage equal to ground, a floating negative supply scheme detailed in Fig. 2 should be used.

For the best performance, the external 50*Ohm* terminations for the outputs should be connected to vcc, but not to ground!

Different PCB layouts will be needed for each different power supply combination.

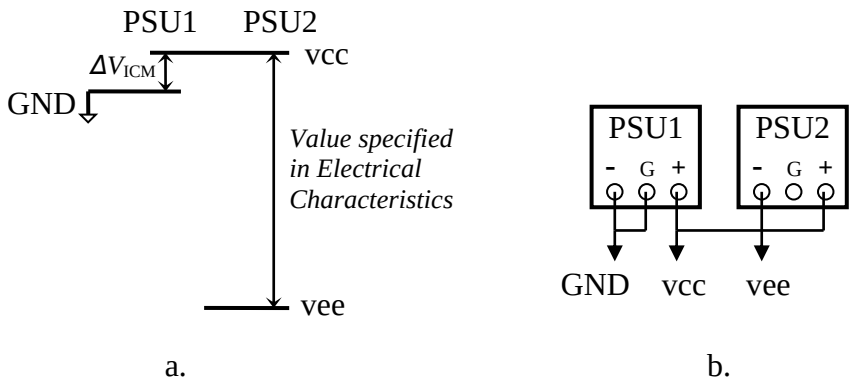

Fig. 2. Floating Negative Supply Scheme: Potential Diagram (a) and Schematic (b)

All the characteristics detailed below assume vcc = 0.0*V* = ground.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

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Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-5.5	*V*
Power Consumption		2.6	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTION

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-speed Signals			
d0p	24	CML - type	Differential high speed data inputs with internal SE 50*Ohm* termination to vcc
d0n	26		
d1p	29	CML - type	
d1n	31		
d2p	2	CML - type	
d2n	4		
d3p	7	CML - type	
d3n	9		
qp	18	CML - type	Differential high speed data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
qn	15		
Control Signals			
lvlcrl	11	CMOS	Required input voltage range selector for sel0/sel1 ports (active: high, voltage range from vee to vee+3.3*V*; default: low or n/c, voltage range from vcc-3.3*V* to vcc)
sel1	37	SE	High-speed input with selectable logic levels, (active: low; default: high). For the selection logic see Table 2
sel0	40	SE	
gncrl0	35	CMOS	Low-speed input with internal 10*KOhm* termination to vcc. For the control logic see Table 1
gncrl1	42	CMOS	
gncrl2	13	CMOS	
gncrl3	20	CMOS	

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply rail	1, 3, 5, 6, 8, 10, 12, 14, 16, 17, 19, 21, 23, 25, 27, 28, 30, 32, 34, 36, 38, 39, 41, 43
vee	Negative power supply rail	22, 33, 44

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-4.7	-4.5	-4.3	*V*	±4.5%
vcc		0.0		*V*	External ground
*I*vee		475		*mA*	
Power consumption		2140		*mW*	
Junction temperature	-25	50	125	*°C*	
Input Analog (d0p/d0n, d1p/d1n, d2p/d2n, d3p/d3n)					
Bandwidth	DC		17	*GHz*	-3*dB*
Common mode level	vcc-0.65	vcc-0.55	vcc-0.45	*mV*	
Input Noise Density		1.5		*nV*/sqrt(*Hz*)	
S11		-30		*dB*	at 1*GHz*
		-8		*dB*	at 20*GHz*
Output Analog (qp/qn)					
Bandwidth	DC		17	*GHz*	-3*dB*
Common mode level		vcc-0.55		*V*	With external 50*Ohm* DC termination to vcc
S22		-27		*dB*	at 1*GHz*
Small Signal Differential Gain	-2.0	0.0	+2.0	*dB*	
Output referred 1*dB* Compression Point		0		*dBm*	Single-Ended, 25*GHz*
2nd harmonic		-55		*dBc*	at 1*GHz*
		-35		*dBc*	at 20*GHz*
3rd harmonic		-55		*dBc*	at 1*GHz*
		-40		*dBc*	at 20*GHz*
Low-Speed Controls (lvlcrl, gncrl 0/1/2/3)					
High logic level		vcc		*V*	
Low logic level		vee		*V*	
High-Speed Control (sel1, sel2)					
Bandwidth		1		*GHz*	
High logic level		vcc		*V*	
Low logic level		vcc-3.3		*V*	-2.4*V* default state
Input current			10	*uA*	sink or source

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DIE INFORMATION

The main dimensions of the die are given in Table 4.

Table 4. Important Die Dimensions

Pad metal dimensions	74μm x 80μm
Pad opening dimensions	68μm x74μm
Die dimensions	1200μm x 1200μm

The part's die incorporates wire bonding pads with the coordinates of their centers given in Table 5.

Table 5. Die Pad Coordinates

Pad Number	X Coordinate, μm	Y Coordinate, μm	Pad Number	X Coordinate, μm	Y Coordinate, μm
1	222	57	23	978	1143
2	306	57	24	894	1143
3	390	57	25	810	1143
4	474	57	26	726	1143
5	558	57	27	642	1143
6	642	57	28	558	1143
7	726	57	29	474	1143
8	810	57	30	390	1143
9	894	57	31	306	1143
10	978	57	32	222	1143
11	1080	120	33	120	1080
12	1143	222	34	57	978
13	1143	306	35	57	894
14	1143	390	36	57	810
15	1143	474	37	57	726
16	1143	558	38	57	642
17	1143	642	39	57	558
18	1143	726	40	57	474
19	1143	810	41	57	390
20	1143	894	42	57	306
21	1143	978	43	57	222
22	1080	1080	44	120	120

The part's identification label is ASNT6161-BD. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 2 characters after the dash indicate that the die is not packaged.

The IC complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all 6 substances.

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REVISION HISTORY

Revision	Date	Changes
1.0.1	11-2017	First release