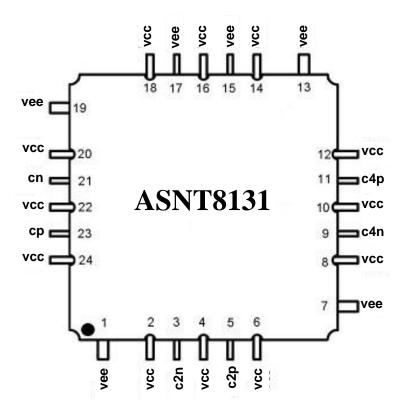
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ASNT8131-KMC 32*GHz* High-Sensitivity Divider by 2 and by 4

- Wide frequency range from DC to 32GHz
- Divided-by-2 and divided-by-4 outputs
- 50% duty cycle of the divided clock signals
- Fully differential CML input interface
- Fully differential CML output interfaces
- Single +3.3V or -3.3V power supply
- Industrial temperature range
- Power consumption of 315mW at full operational speed
- Custom CQFP 24-pin package



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DESCRIPTION

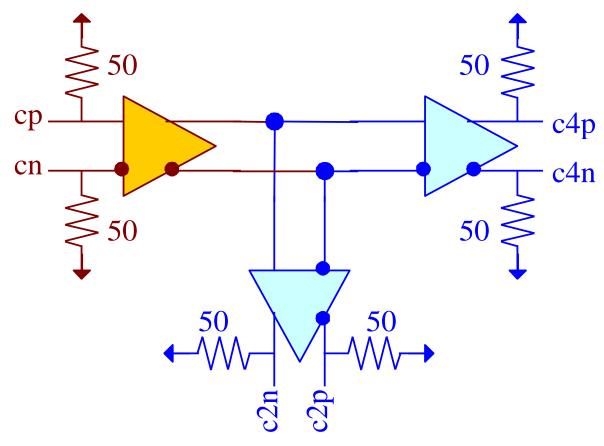


Fig. 1. Functional Block Diagram

ASNT8131-KMC is a high-speed, low-power divider by-2 and by-4 with increased sensitivity. The part shown in Fig. 1 accepts a CML input clock signal cp/cn with the speed from DC to maximum operational frequency and provides clean 50% duty cycle output signals with divided-by-2 c2p/c2n and divided-by-4 c4p/c4n frequency.

The part's I/Os support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in **Error! Reference source not found.** In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0V = ground and vee = -3.3V), or a positive supply (vcc = +3.3V and vee = 0.0V = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50Ohm termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0V and vee = -3.3V.



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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in *Table 1* may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		0.35	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	$^{\circ}C$
Storage Temperature	-40	+100	$^{\circ}C$
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TE	RMIN	A L	DESCRIPTION			
Name	No.	Type				
	High-Speed I/Os					
ср	23	CML	Differential clock input with internal SE 50 <i>Ohm</i> termination to			
cn	21	input	VCC			
c2p	5	CML	Differential divided of	clock outputs with internal SE 500hm		
c2n	3	output	termination to vcc. Re	equire external SE 50 <i>Ohm</i> termination to		
c4p	11		VCC			
c4n	9					
Supply and Termination Voltages						
Name	Description		escription	Pin Number		
vcc	vcc Positive power supply $(+3.3V \text{ or } 0V)$		supply (+3.3 <i>V</i> or 0 <i>V</i>)	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24		
vee	Negative power supply (0 <i>V</i> or -3.3 <i>V</i>)		r supply (0 <i>V</i> or -3.3 <i>V</i>)	1, 7, 13, 15, 17, 19		



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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS	
General Parameters						
vee	-3.1	-3.3	-3.5	V	±6%	
VCC		0.0		V	External ground	
<i>I</i> vee		95		mА		
Power consumption		315		mW		
Junction temperature	-25	50	125	$^{\circ}C$		
HS Input Clock (cp/cn)						
Frequency	0		32	GHz		
Swing	40		800	mV	Differential or SE, p-p	
CM Voltage Level	vcc-0.8	vcc-0.2	VCC	mV	Must match for both inputs	
Output Divided Clock (c2p/c2n, c4p/c4n)						
Frequency f/2	0		16	GHz	For c2 out signal	
Frequency f/4	0		8	GHz	For c4 out signal	
Logic "1" level		VCC		V		
Logic "0" level	١	/cc-0.35		V	With external 50 <i>Ohm</i> DC termination	
Duty cycle	45	50	55	%		
Additive Jitter		TBD		ps	Peak-to-peak	

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the **vcc** plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT8131-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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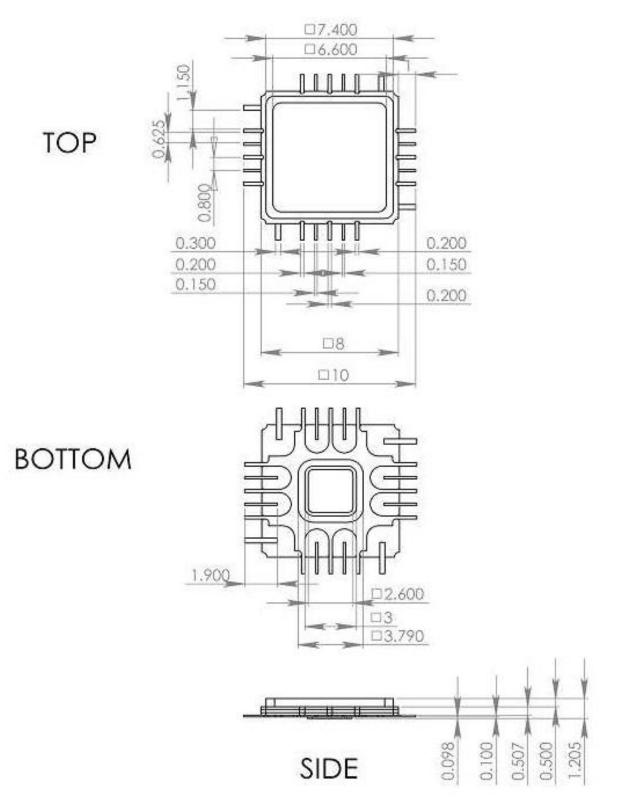


Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)



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REVISION HISTORY

Revision	Date	Changes		
1.2.2	02-2020	Updated Package Information		
1.1.2	07-2019	Updated Letterhead		
1.1.1	12-2016	Corrected package type		
		Corrected description		
		Corrected specification of the output swing		
1.0.1	12-2016	First release		