ADSANTEC
Ultra High-Speed Mixed Signal ASICs

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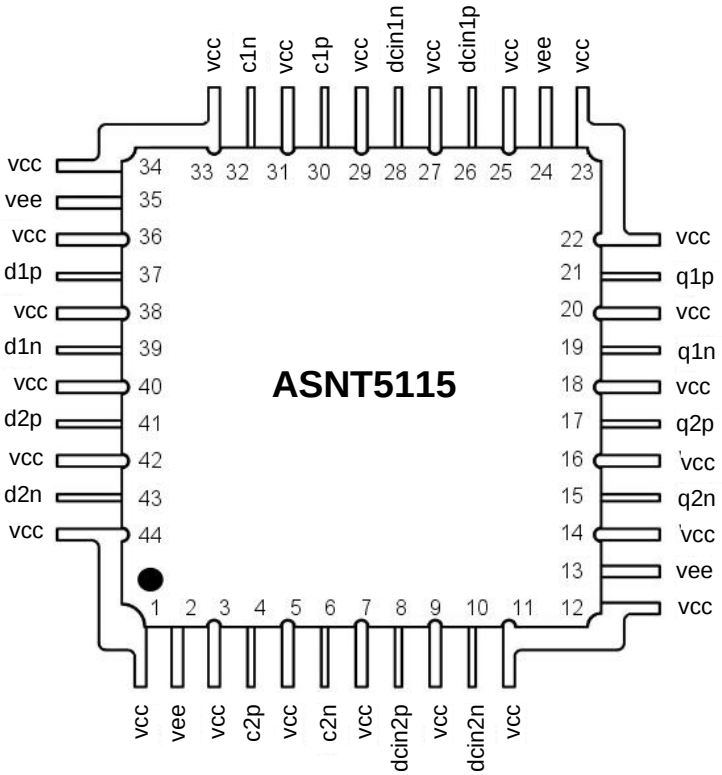
# ASNT5115-KMM
# High Sensitivity DC-to-32*Gbps* Dual D-Type Flip-Flop

- High speed broadband 2-channel D-Type Flip-Flop for data retiming with full rate clock
- Additional input buffer / level shifter for improved protection
- Sensitive input data buffer with increased CM range that is ideal for sampling applications
- Input data single-ended common mode controls
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 4*ps* set-up/hold time capability
- 88% clock phase margin for retiming of data input eye
- Fully differential CML input interfaces
- Fully differential CML output interface with 400*mV* single-ended swing
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 1.02*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 44-pin package



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# DESCRIPTION

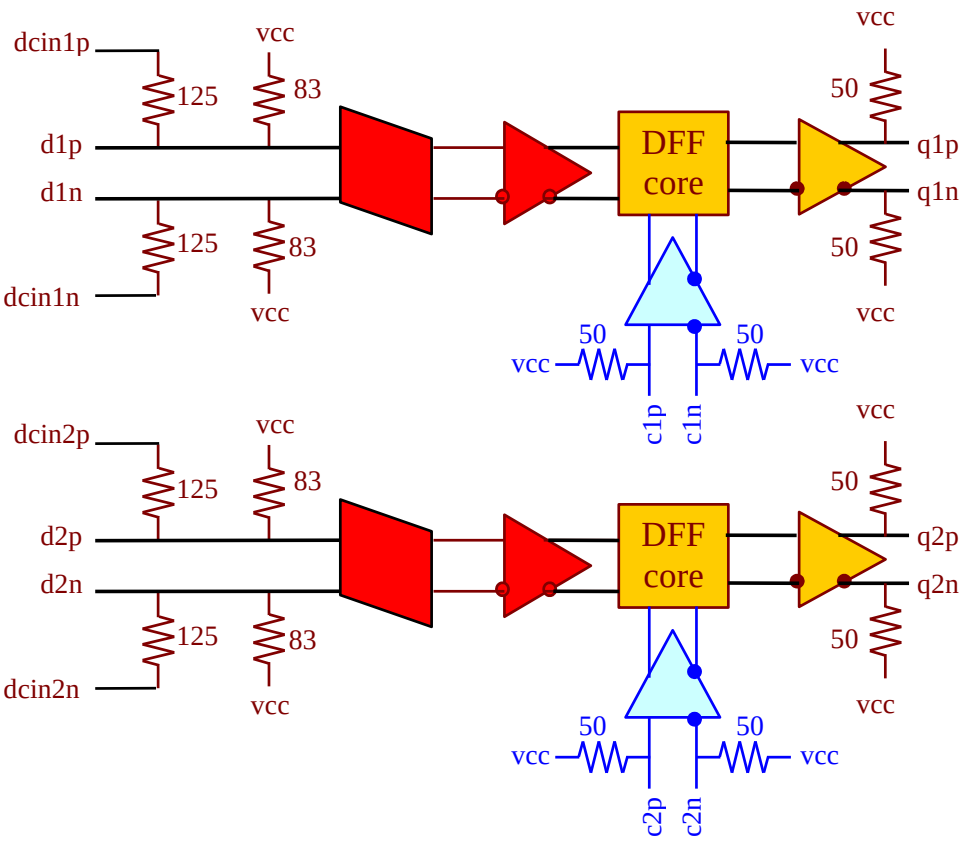


*Fig. 1. Functional Block Diagram*

The temperature stable ASNT5115-KMM SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. The dual-channel IC shown in Fig. 1 can sample up to 32*Gbps* data signals d1p/d1n and d2p/d2n with up to 32*GHz* clock sources c1p/c1n and c2p/c2n to create 32*Gbps* retimed NRZ data outputs q1p/q1n and q2p/q2n. The data input buffers are designed to have increased input signal sensitivity and are able to operate over a wider range of input common mode (CM) voltages. The actual common mode voltage levels on data inputs d1p/d1n and d2p/d2n can be adjusted by applying voltages between vee and vcc to the corresponding control inputs dcin1p/dcin1n and dcin2p/dcin2n.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

It should be noted that control inputs dcin1p/dcin1n and dcin2p/dcin2n should be always connected to voltage sources to ensure correct 50*Ohm* terminations for the data inputs.

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# POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

**All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.**

# ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

*Table 1. Absolute Maximum Ratings*

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply Voltage (vee) | | -3.6 | *V* |
| Power Consumption | | 1.2 | *W* |
| Input Data Voltage Swing (SE) | | 1.7 | *V* |
| Input Clk Voltage Swing (SE) | | 1.7 | *V* |
| Case Temperature | | +90 | *ºC* |
| Storage Temperature | -40 | +100 | *ºC* |
| Operational Humidity | 10 | 98 | *%* |
| Storage Humidity | 10 | 98 | *%* |

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# TERMINAL FUNCTIONS

| TERMINAL | | | DESCRIPTION |
|---|---|---|---|
| **Name** | **No.** | **Type** | |
| **High-Speed I/Os** | | | |
| d1p | 37 | CML Input | Differential data inputs with internal SE 50*Ohm* termination to vcc |
| d1n | 39 | | |
| d2p | 41 | | |
| d2n | 43 | | |
| c1p | 30 | CML Input | Differential clock inputs with internal SE 50*Ohm* termination to vcc |
| c1n | 32 | | |
| c2p | 4 | | |
| c2n | 6 | | |
| q1p | 21 | CML Output | Differential data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc |
| q1n | 19 | | |
| q2p | 17 | | |
| q2n | 15 | | |
| **DC Controls** | | | |
| dcin1p | 26 | Input | Input data DC common mode voltage level controls. **Should be always connected to voltage sources!** |
| dcin1n | 28 | | |
| dcin2p | 8 | | |
| dcin2n | 10 | | |

| **Supply and Termination Voltages** | | |
|---|---|---|
| **Name** | **Description** | **Pin Number** |
| vcc | Positive power supply (+3.3*V* or 0*V*) | 1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 23, 25, 27, 29, 31, 33, 34, 36, 38, 40, 42, 44 |
| vee | Negative power supply (0*V* or -3.3*V*) | 2, 13, 24, 35 |

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# ELECTRICAL CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **General Parameters** | | | | | |
| vcc | | 0.0 | | *V* | External ground |
| vee | -3.47 | -3.3 | -3.14 | *V* | ±5% |
| *I*vcc | | 310 | 340 | *mA* | |
| Power consumption | | 1.02 | 1.12 | *W* | |
| Junction temperature | -25 | 50 | 125 | *°C* | |
| **HS Input Data (d1p/d1n, d2p/d2n)** | | | | | |
| Data rate | 0.0 | 32 | 40 | *Gbps* | |
| Swing | 0.01 | | 1.3 | *V* | Differential or SE, p-p |
| CM Voltage Level | vcc-0.7+sw/2 | | vcc+0.6-sw/2 | *V* | Must match for both inputs |
| **HS Input Clock (c1p/c1n, c2p/c2n)** | | | | | |
| Frequency | 0.0 | 32 | 40 | *GHz* | |
| Swing | 0.05 | | 1.3 | *V* | Differential or SE, p-p |
| CM Voltage Level | vcc-0.7+sw/2 | | vcc+0.6-sw/2 | *V* | Must match for both inputs |
| Duty Cycle | 40 | 50 | 60 | *%* | |
| Clock phase margin | 86 | 88 | 90 | *%* | For reliable data latching |
| **HS Output Data (q1p/q1n, q2p/q2n)** | | | | | |
| Data rate | 0.0 | 32 | 40 | *Gbps* | |
| Logic "1" level | vcc-0.05 | vcc-0.03 | vcc-0.01 | *V* | |
| Logic "0" level | vcc-0.46 | vcc-0.44 | vcc-0.42 | *V* | With external 50*Ohm* DC termination |
| Jitter | | 0.15 | | *ps* | Peak-to-peak at 32*Gbps* |
| **DC Input Controls (dcin1p/dcin1n, dcin2p/dcin2n)** | | | | | |
| Max level | | vcc + 1.0 | | *V* | |
| Min level | | vcc - 1.0 | | *V* | |

# PACKAGE INFORMATION

The chip die is housed in a custom 44-pin CQFP package shown in Fig. 2. Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to the vcc plain that is ground for the negative supply or power for the positive supply.

The part's identification label is ASNT5115-KMM. The first 8 characters of the name before the underscore identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

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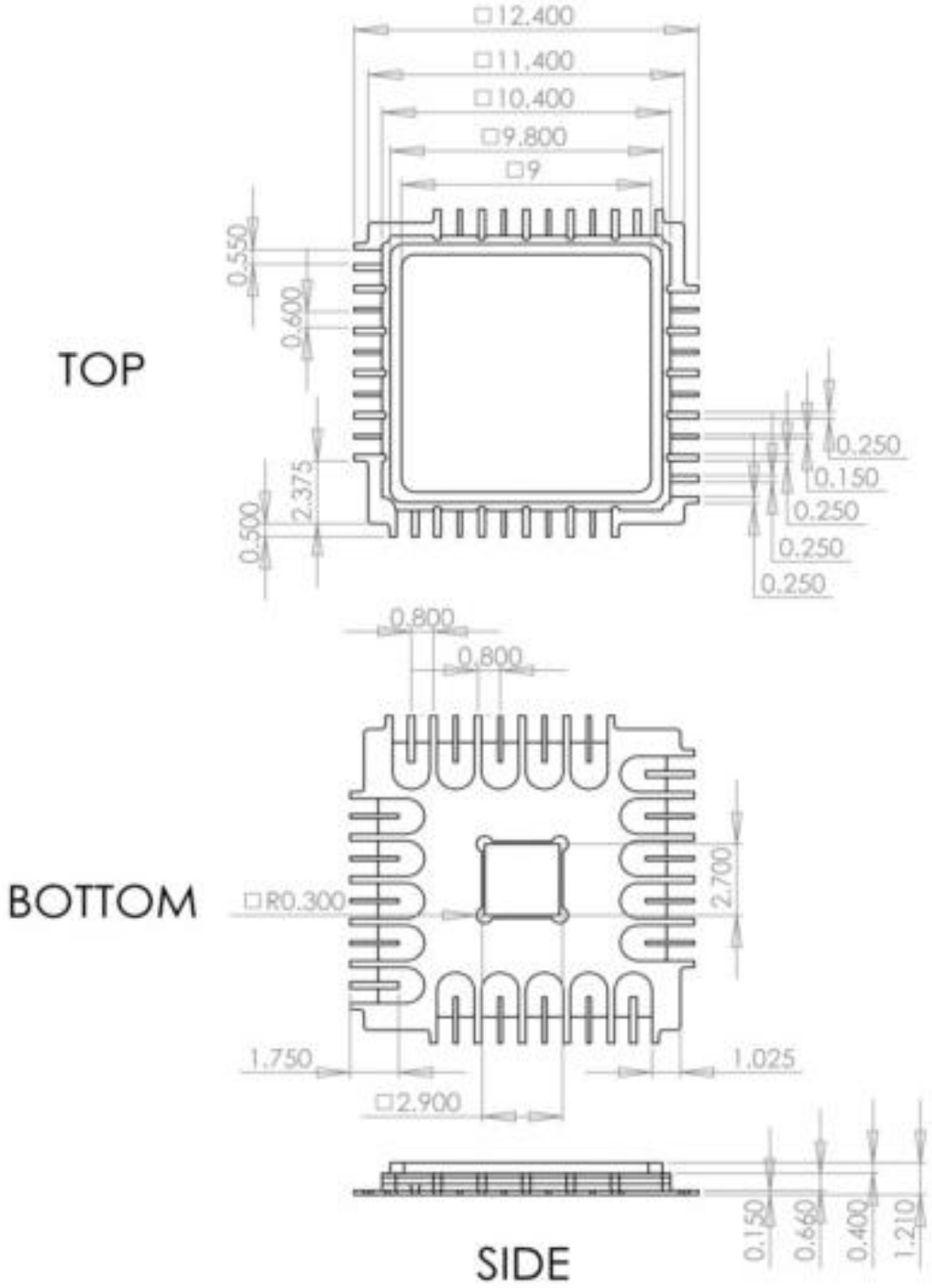


*Fig. 2. CQFP 44-Pin Package Drawing (All Dimensions in mm)*

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# REVISION HISTORY

| Revision | Date | Changes |
|---|---|---|
| 1.2.2 | 07-2019 | Updated Letterhead |
| 1.2.1 | 05-2013 | Removed data duty cycle specification<br>Corrected terminal functions |
| 1.1.1 | 05-2013 | Corrected pin out diagram |
| 1.0.1 | 03-2013 | First release |