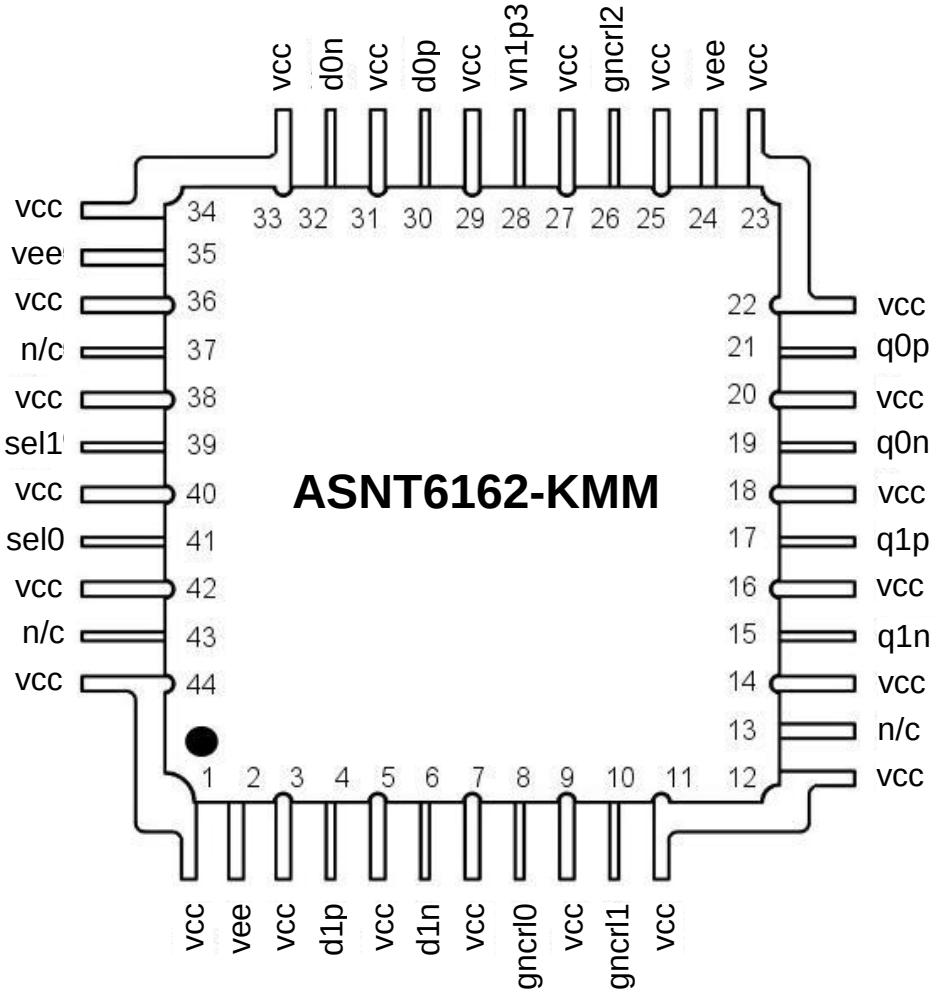
ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

ASNT6162-KMM
DC-17*GHz* Linear Non-Blocking Cross-Switch 2x2

- DC to 17*GHz* broadband operation
- Two differential CML-type input ports and two differential CML-type output ports
- Temperature-stabilized differential gain of approximately 0*dB*
- 1*dB* compression point of 0*dBm*
- DC-to-1*GHz* broadband channel selector ports
- Low jitter and limited temperature variation over industrial temperature range
- Single +4.5*V* or -4.5*V* power supply
- Power consumption: 1260*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 44-pin package



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DESCRIPTION

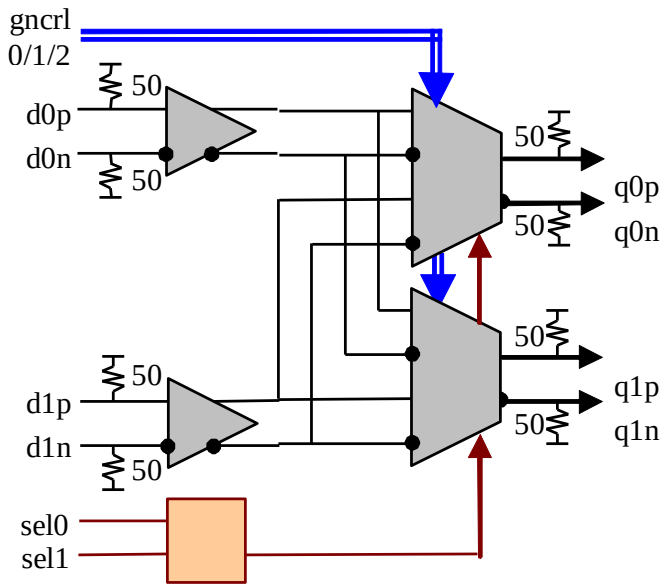

Fig. 1. Functional Block Diagram

The temperature stable ASNT6162-KMM linear non-blocking cross-switch 2x2 is intended for use in high-speed systems. The IC shown in Fig. 1 can deliver two different broad-band analog differential signals d0p/d0n and d1p/d1n to two differential outputs q0p/q0n and q1p/q1n with a nominal gain of 0*dB*. The gain can be fine-tuned using the 3-pin control port gncrl0/1/2 with accuracy of 0.5*dB* as shown in Table 1.

Table 1. Gain Control

gncrl2	gncrl1	gncrl0	Gain, *dB*	Comments
0	0	0	-1.0	
0	0	1	-0.5	
0	1	0	-0.5	
0	1	1	0	default state
1	0	0	0.5	
1	0	1	0.5	
1	1	0	1.0	
1	1	1	1.0	

The assignment of inputs to outputs is performed through the external high-speed dual port sel1/sel2 that is referenced to vcc. The assignment logic is shown in Table 2.

Table 2. Channel Selection

sel1	sel0	Input connected to q0	Input connected to q1	Comments
0	0	d0	d0	default state
0	1	d1	d0	
1	0	d0	d1	
1	1	d1	d1	

The part's I/Os support the CML-type interface with on chip 50*Ohm* termination to vcc, and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance. In particular, the specified output common-mode voltage level is guaranteed only in case of external single-ended 50*Ohm* DC termination to vcc.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V* = ground), or a positive supply (vee = 0.0*V* = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. In any case, the input common mode voltage level is shifted down from vcc by a certain voltage of ΔV_{ICM} as specified in ELECTRICAL CHARACTERISTICS. To have the input common mode voltage equal to ground, a floating negative supply scheme detailed in Fig. 2 should be used.

For the best performance, the external 50*Ohm* terminations for the outputs should be connected to vcc, but not to ground!

The part features an additional internal supply voltage vn1p3 that is also accessible through the corresponding pin. This pin is recommended to be left not connected but can be also used for adjustment of the output eye by applying an external voltage source within the range specified in ELECTRICAL CHARACTERISTICS. The external supply should be able to both source and sink a current of about 1*mA*.

Different PCB layouts will be needed for each different power supply combination.

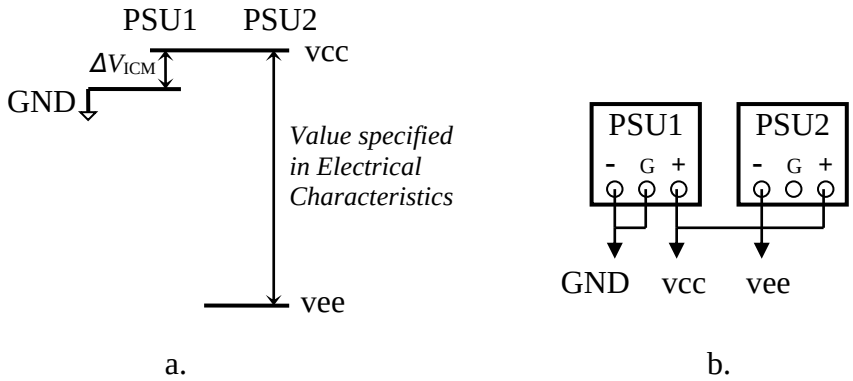

Fig. 2. Floating Negative Supply Scheme: Potential Diagram (a) and Schematic (b)

All the characteristics detailed below assume vcc = 0.0*V* = ground.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the

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absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-5.5	*V*
Power Consumption		1.5	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTION

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-speed Signals			
d0p	30	CML - type	Differential high speed data inputs with internal SE 67*Ohm* termination to vcc and SE 50*Ohm* termination to virtual ground
d0n	32		
d1p	4	CML - type	
d1n	6		
q0p	21	CML - type	Differential high speed data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
q0n	19		
q1p	17	CML - type	
q1n	15		
Control Signals			
sel0	41	SE	High-speed input with selectable logic levels, (active: high; default: low). For the selection logic see Table 2
sel1	39	SE	
gncrl0	8	CMOS	Low-speed input with internal 10*KOhm* termination to vcc. For the control logic see Table 1
gncrl1	10	CMOS	
gncrl2	26	CMOS	Low-speed input with internal 10*KOhm* termination to vee. For the control logic see Table 1

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply rail	1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 23, 25, 27, 29, 31, 33, 34, 36, 38, 40, 42, 44
vee	Negative power supply rail	2, 24, 35
vn1p3	Internal supply vcc-1.3*V*	28
n/c	Not connected pins	13, 37, 43

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-4.7	-4.5	-4.3	*V*	±4.5%
vcc		0.0		*V*	External ground
*I*vee		280		*mA*	
Power consumption		1260		*mW*	
Junction temperature	-25	50	125	*°C*	
Input Analog (d0p/d0n, d1p/d1n)					
Bandwidth	DC		17	*GHz*	-3*dB*
Common mode level	vcc-0.6	vcc-0.5	vcc-0.4	*mV*	
Input Noise Density		1.5		*nV*/sqrt(*Hz*)	
S11		-30		*dB*	at 1*GHz*
		-8		*dB*	at 20*GHz*
Output Analog (q0p/q0n, q1p/q1n)					
Bandwidth	DC		17	*GHz*	-3*dB*
Common mode level		vcc-0.55		*V*	With external 50*Ohm* DC termination to vcc
S22		-27		*dB*	at 1*GHz*
Small Signal Differential Gain	-1.0	0.0	+1.0	*dB*	
Output referred 1*dB* Compression Point		0		*dBm*	Single-Ended, 20*GHz*
2nd harmonic		-55		*dBc*	at 1*GHz*
		-35		*dBc*	at 20*GHz*
3rd harmonic		-55		*dBc*	at 1*GHz*
		-40		*dBc*	at 20*GHz*
Low-Speed Controls (gncrl 0/1/2)					
High logic level		vcc		*V*	
Low logic level		vee		*V*	
High-Speed Control (sel0, sel1)					
Bandwidth		1		*GHz*	
High logic level		vcc		*V*	
Low logic level		vcc-3.3		*V*	-2.4*V* default state
Input current			10	*uA*	sink or source
Additional Internal Supply (vn1p3)					
Nominal voltage value		vcc-1.3		*V*	when not connected
Adjustment range	vcc-1.6		vcc-1.0	*V*	with external supply
Current			1	*mA*	source or sink

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PACKAGE INFORMATION

The chip die is housed in a custom 44-pin CQFP package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT6162-KMM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

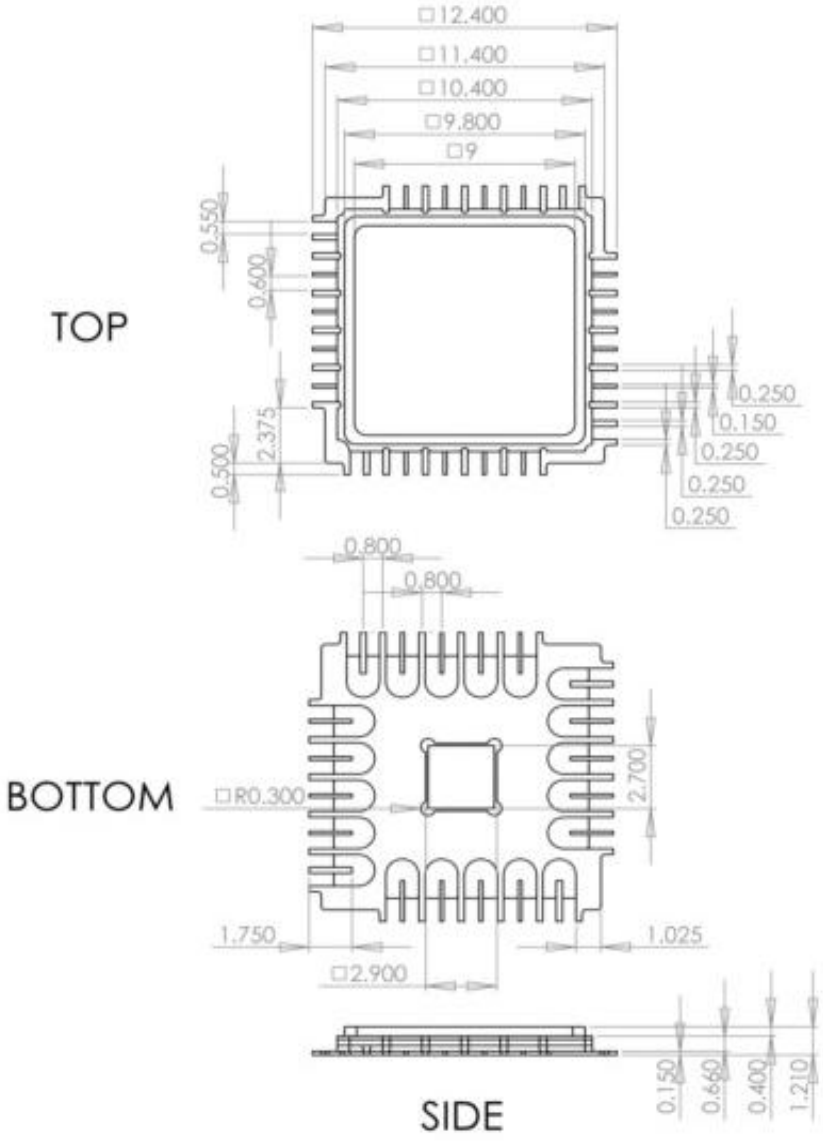

Fig. 3. CQFP 44-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.3.2	07-2019	Updated Letterhead
1.3.1	05-2018	Corrected the maximum frequency of operation
1.2.1	04-2018	Added description of the vn1p3 pin (updated description, Terminal Functions, and Electrical characteristics)
1.1.1	08-2017	Corrected power supply value
1.0.1	08-2017	First release Corrected description
0.2.1	08-2017	Corrected pin out diagram Removed lvlcrl pin and its description Corrected bandwidth
0.1.1	07-2017	Pin name sel2 was changed to sel0 in description tables and in the block diagram. Channel selection table was corrected.
0.0.1	08-2016	Preliminary release