ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
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ASNT8132-MOD
DC-54*GHz* Broadband Clock Divider by 2

- High speed broadband clock divider by 2
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Fully differential CML input interface
- Fully differential CML output interface with 400*mV* single-ended swing
- Single -3.3*V* power supply
- Power consumption: 630*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom module solution from Marki Microwave

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DESCRIPTION

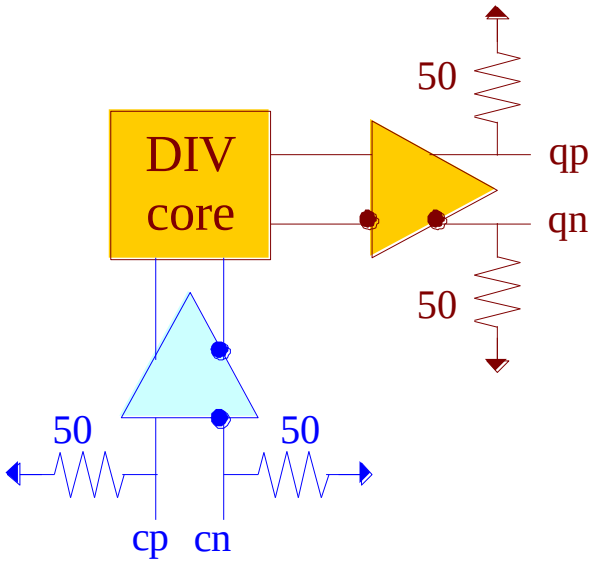

Fig. 1. Functional Block Diagram

The temperature stable ASNT8132-MOD SiGe IC provides broadband clock divide-by-2 functionality, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can process a high-speed clock input signal cp/cn and deliver a half rate clock output signal qp/qn with 50% duty cycle.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part operates from a single negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*) configuration.

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		0.7	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
cp	2	CML input	Differential clock inputs with internal SE 50*Ohm* termination to vcc
cn	3		
qp	6	CML output	Differential clock outputs with internal SE 50*Ohm* termination to vcc.
qn	5		

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (0*V*)	1, 8
vee	Negative power supply (-3.3*V*)	4, 7

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		190		*mA*	
Power consumption		630		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Clock (cp/cn)					
Frequency	DC		54	*GHz*	
Swing	0.2		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output Clock (qp/qn)					
Frequency	DC		27	*GHz*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.4		*V*	With external 50*Ohm* DC termination
Rise/Fall times	4	5	7	*ps*	20%-80%
Output Jitter			1	*ps*	Peak-to-peak
Duty cycle	45	50	55	*%*	

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PACKAGE INFORMATION

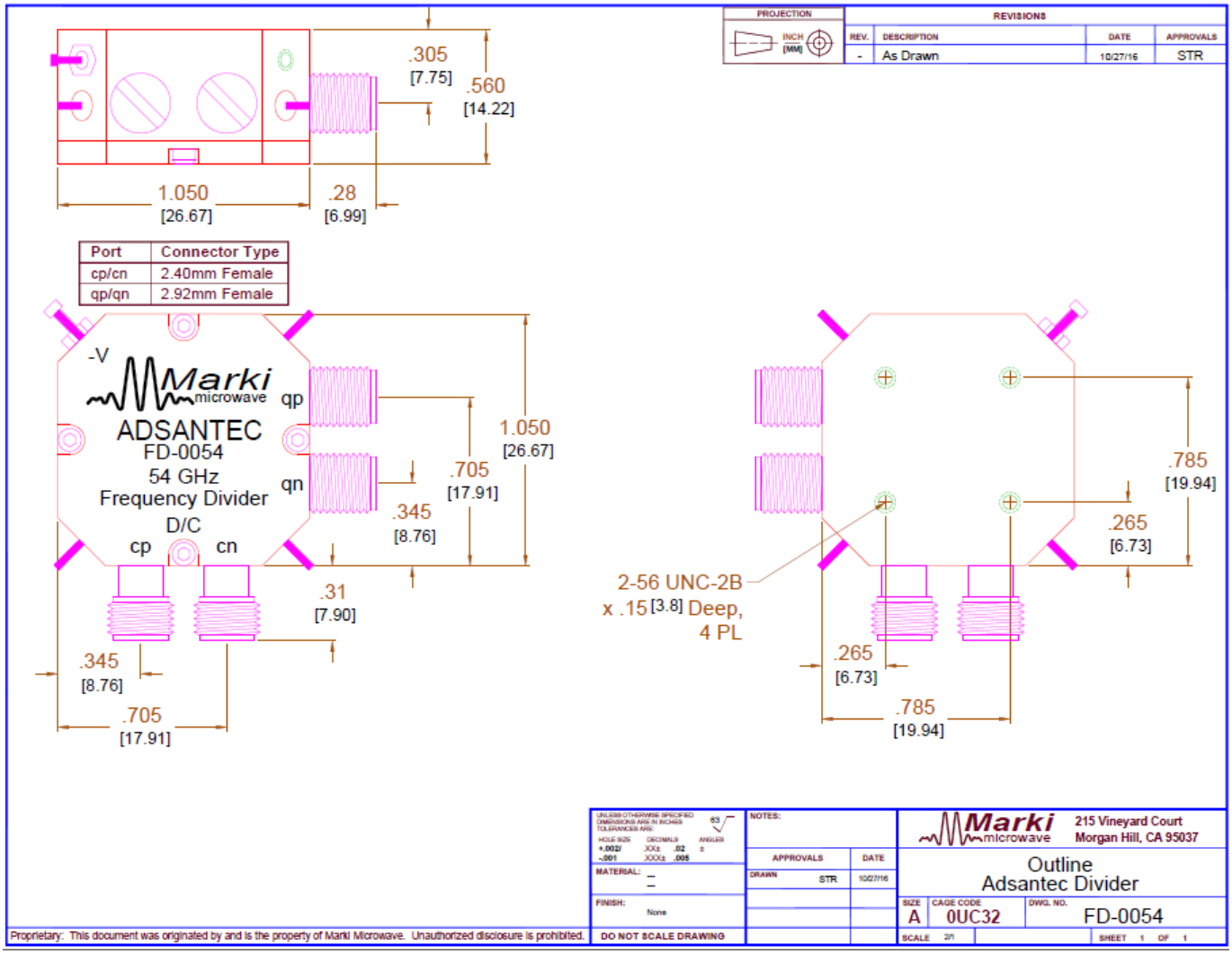

Fig. 2. Module Mechanical Dimensions mm [inches]

REVISION HISTORY

Revision	Date	Changes
1.0.2	07-2019	Updated Letterhead
1.0.1	02-2019	First release